FIG. 1A

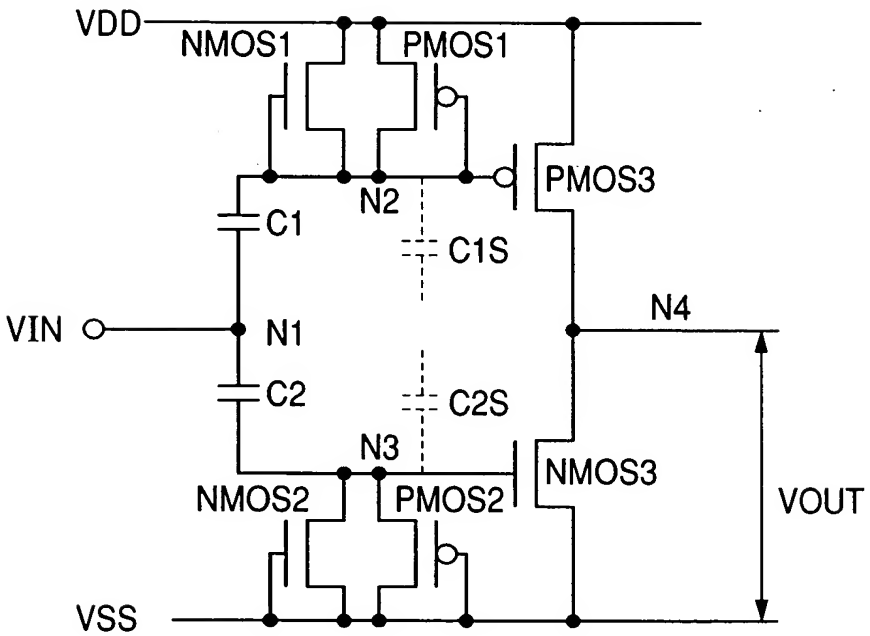
VDD
NMOS1
PMOS1
PMOS3
N2
C1
C1S
VIN
N1
N4
C2
C2S
N3
NMOS3
NMOS2
PMOS2
VOUT
VSS

FIG. 1B

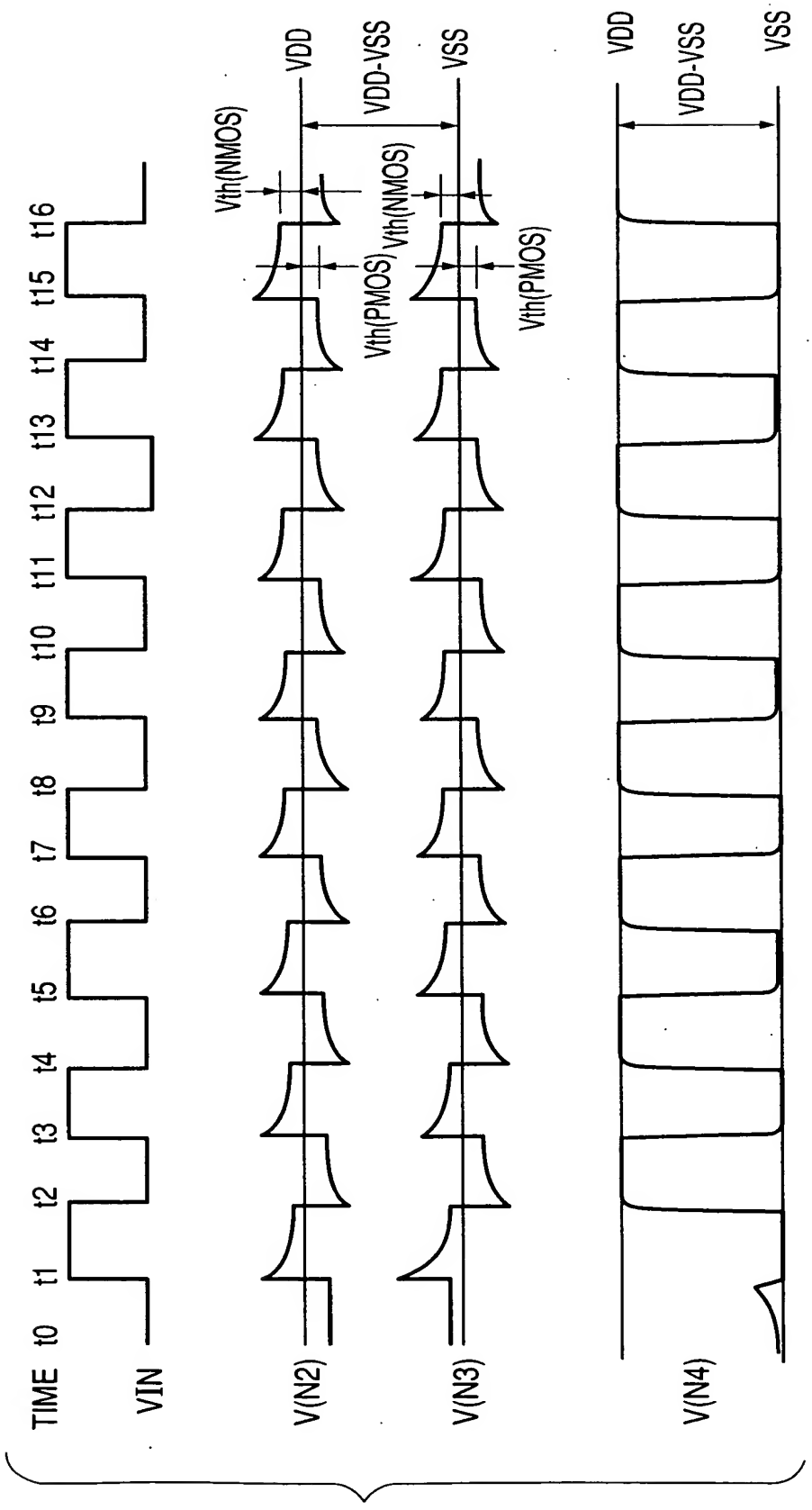
TIME
t0
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12
t13
t14
t15
t16
VIN
V(N2)
V(N3)
V(N4)
VDD
VDD-VSS
VSS
Vth(NMOS)
Vth(PMOS)
Vth(NMOS)
Vth(PMOS)
VDD
VDD-VSS
VSS

FIG. 2

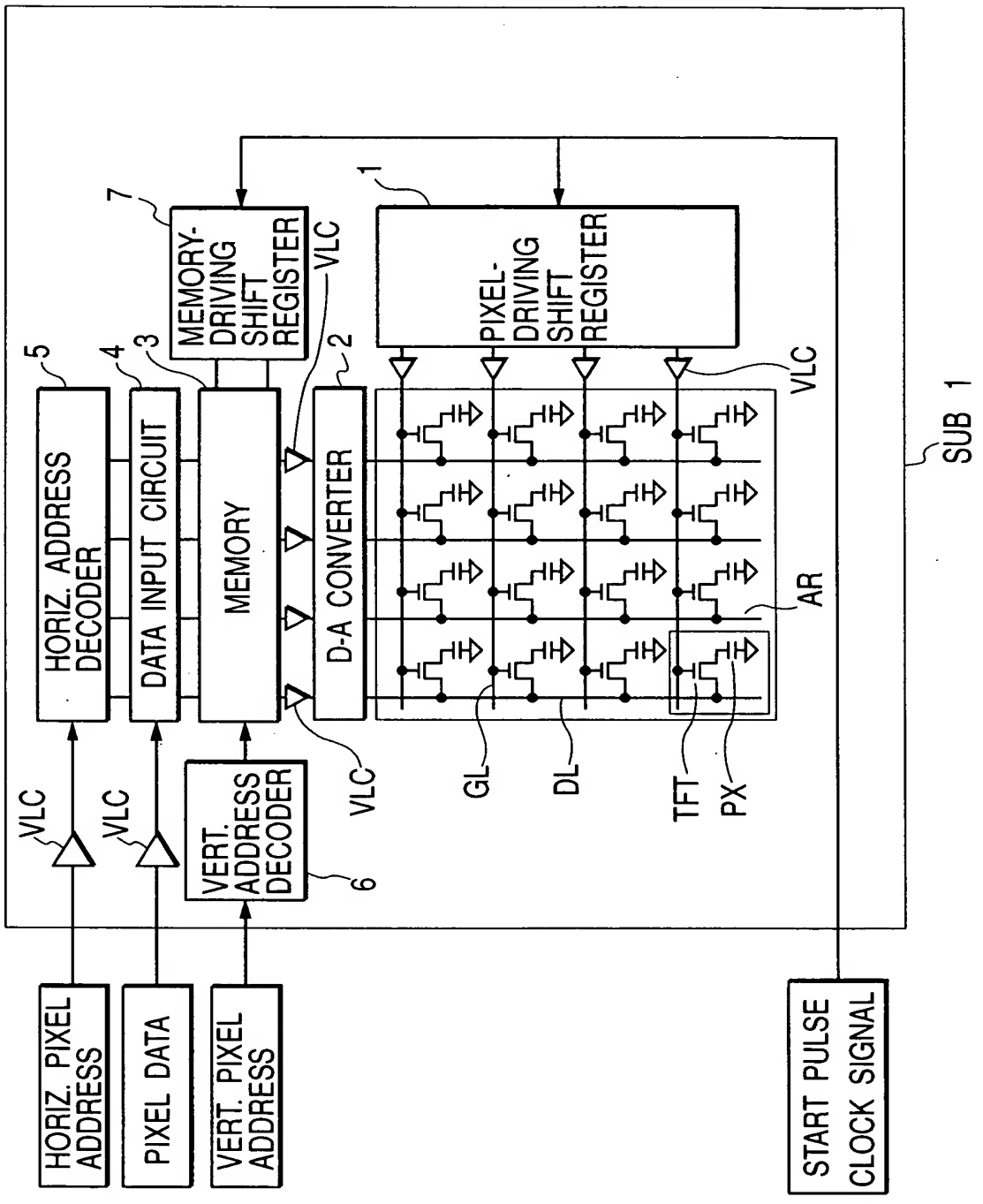
HORIZ. PIXEL ADDRESS
PIXEL DATA
VERT. PIXEL ADDRESS
START PULSE CLOCK SIGNAL
SUB 1
HORIZ. ADDRESS DECODER
DATA INPUT CIRCUIT
MEMORY
D-A CONVERTER
MEMORY-DRIVING SHIFT REGISTER
PIXEL-DRIVING SHIFT REGISTER
VERT. ADDRESS DECODER
VLC
GL
DL
TFT
PX
AR
1
2
3
4
5
6
7

FIG. 3

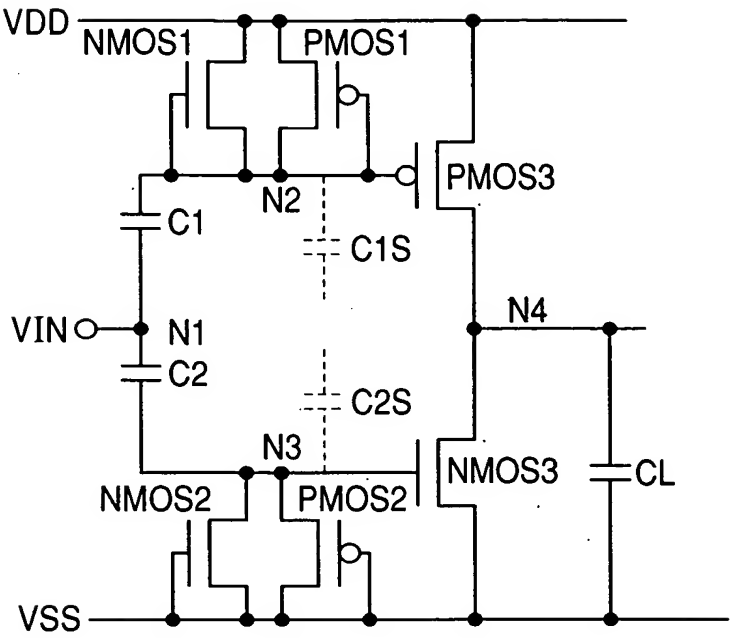
VDD
NMOS1
PMOS1
PMOS3
N2
C1
C1S
VIN
N1
N4
C2
C2S
N3
NMOS3
CL
NMOS2
PMOS2
VSS

FIG. 4A

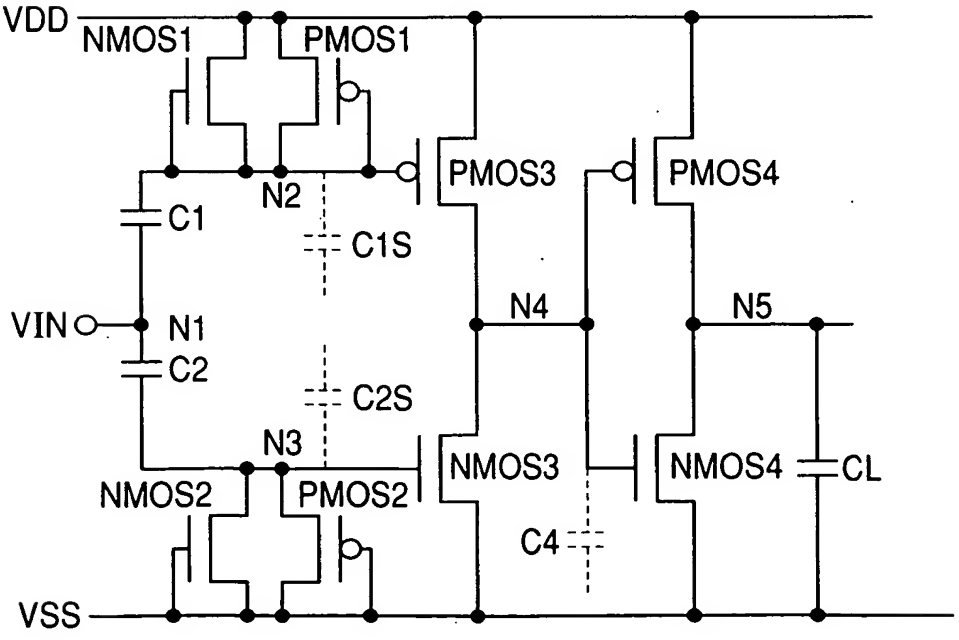
VDD
NMOS1
PMOS1
PMOS3
PMOS4
N2
C1
C1S
N4
N5
VIN
N1
C2
C2S
N3
NMOS3
NMOS4
CL
NMOS2
PMOS2
C4
VSS

FIG. 4B

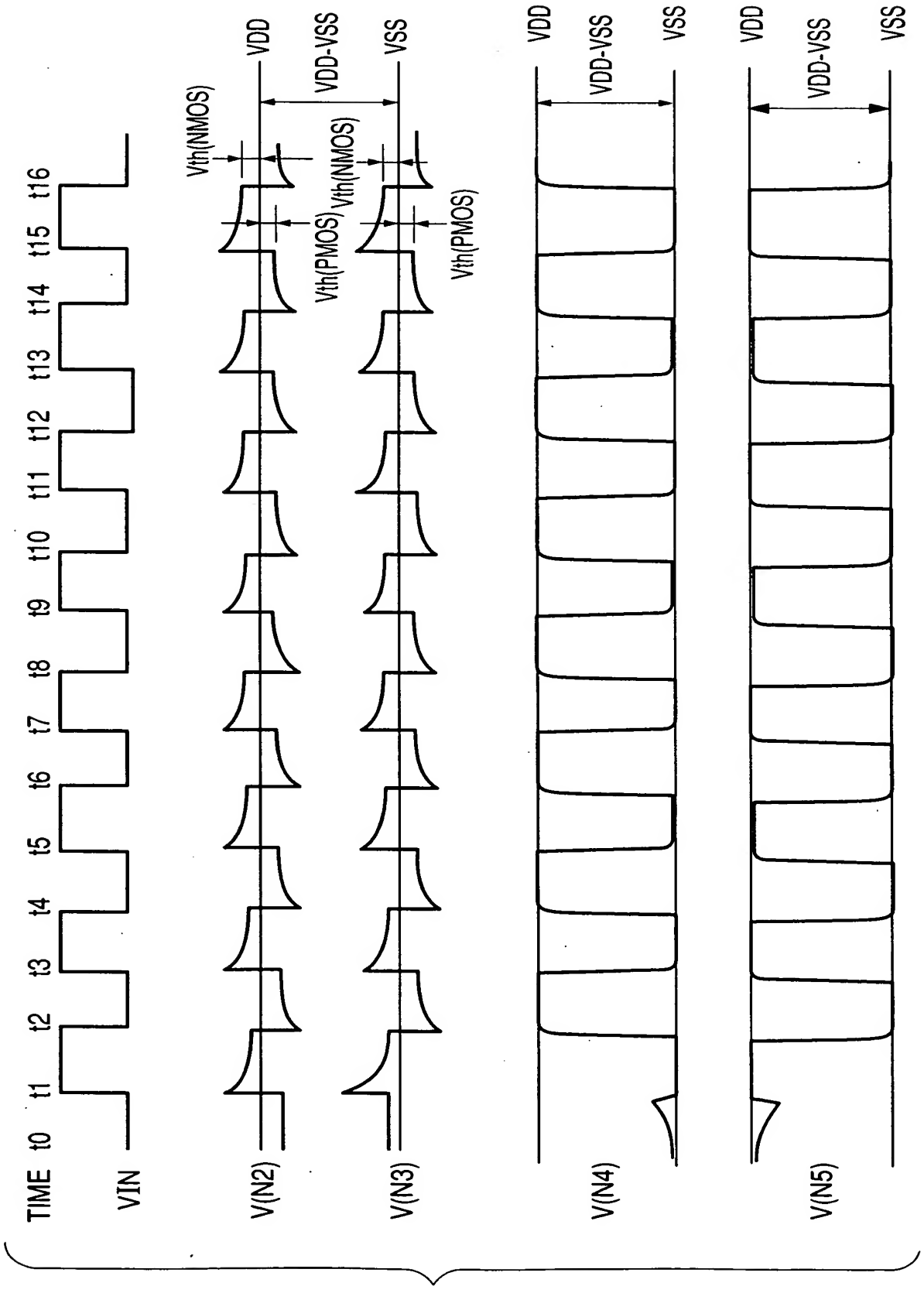
TIME
t0
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12
t13
t14
t15
t16
VIN
V(N2)
V(N3)
V(N4)
V(N5)
VDD
VSS
VDD-VSS
Vth(NMOS)
Vth(PMOS)

FIG. 5

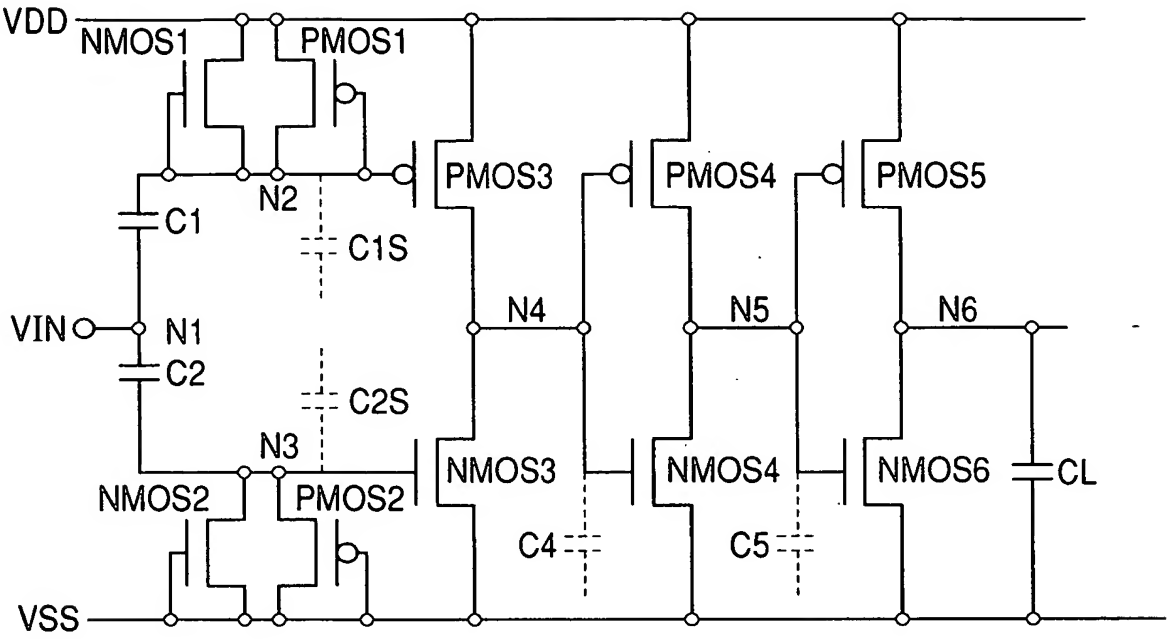
VDD
NMOS1
PMOS1
PMOS3
PMOS4
PMOS5
N2
C1
C1S
VIN
N1
N4
N5
N6
C2
C2S
N3
NMOS3
NMOS4
NMOS6
CL
NMOS2
PMOS2
C4
C5
VSS

FIG. 6

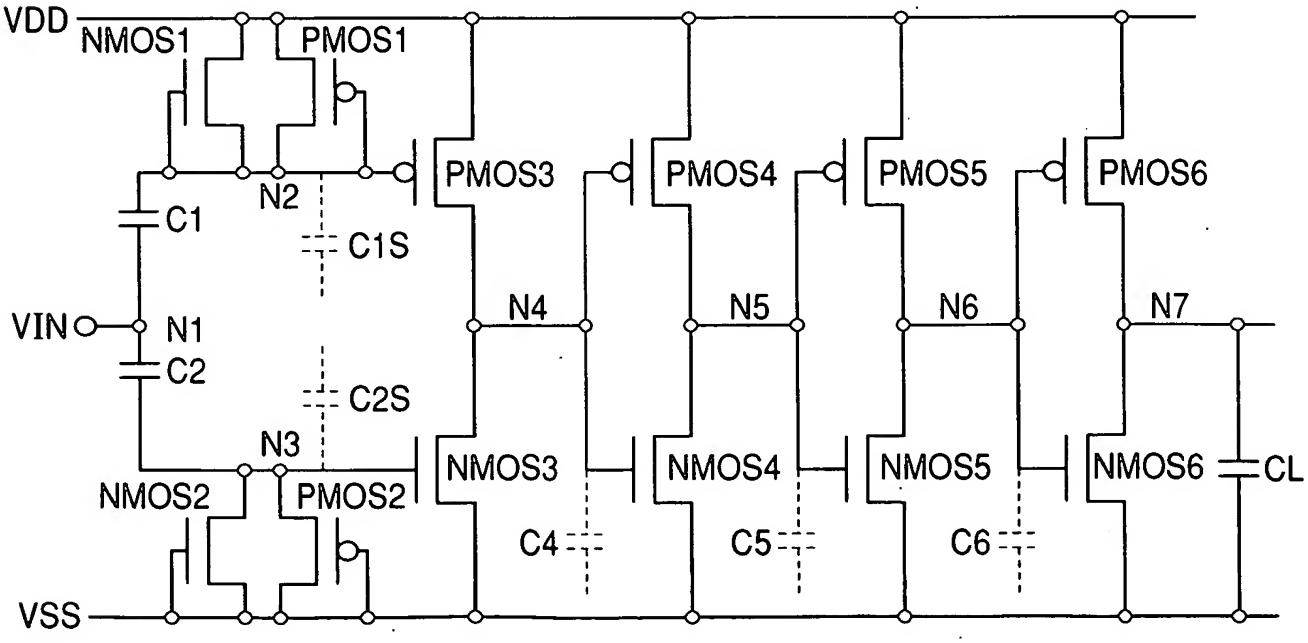
VDD
NMOS1
PMOS1
PMOS3
PMOS4
PMOS5
PMOS6
N2
C1
C1S
VIN
N1
N4
N5
N6
N7
C2
C2S
N3
NMOS3
NMOS4
NMOS5
NMOS6
CL
NMOS2
PMOS2
C4
C5
C6
VSS

FIG. 7A

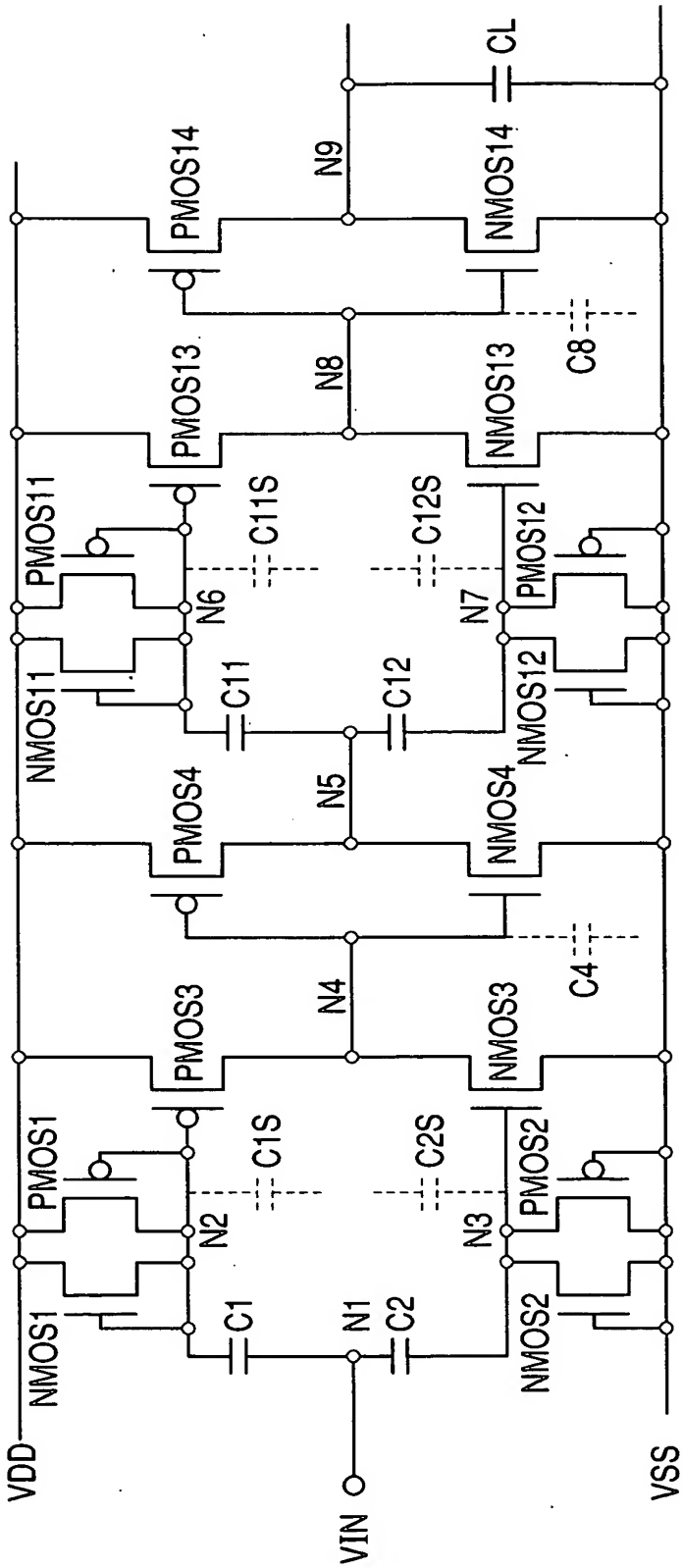
VDD
VSS
VIN
NMOS1
PMOS1
NMOS2
PMOS2
NMOS3
PMOS3
NMOS4
PMOS4
NMOS11
PMOS11
NMOS12
PMOS12
NMOS13
PMOS13
NMOS14
PMOS14
C1
C2
C4
C8
C11
C12
C1S
C2S
C11S
C12S
CL
N1
N2
N3
N4
N5
N6
N7
N8
N9

FIG. 7B

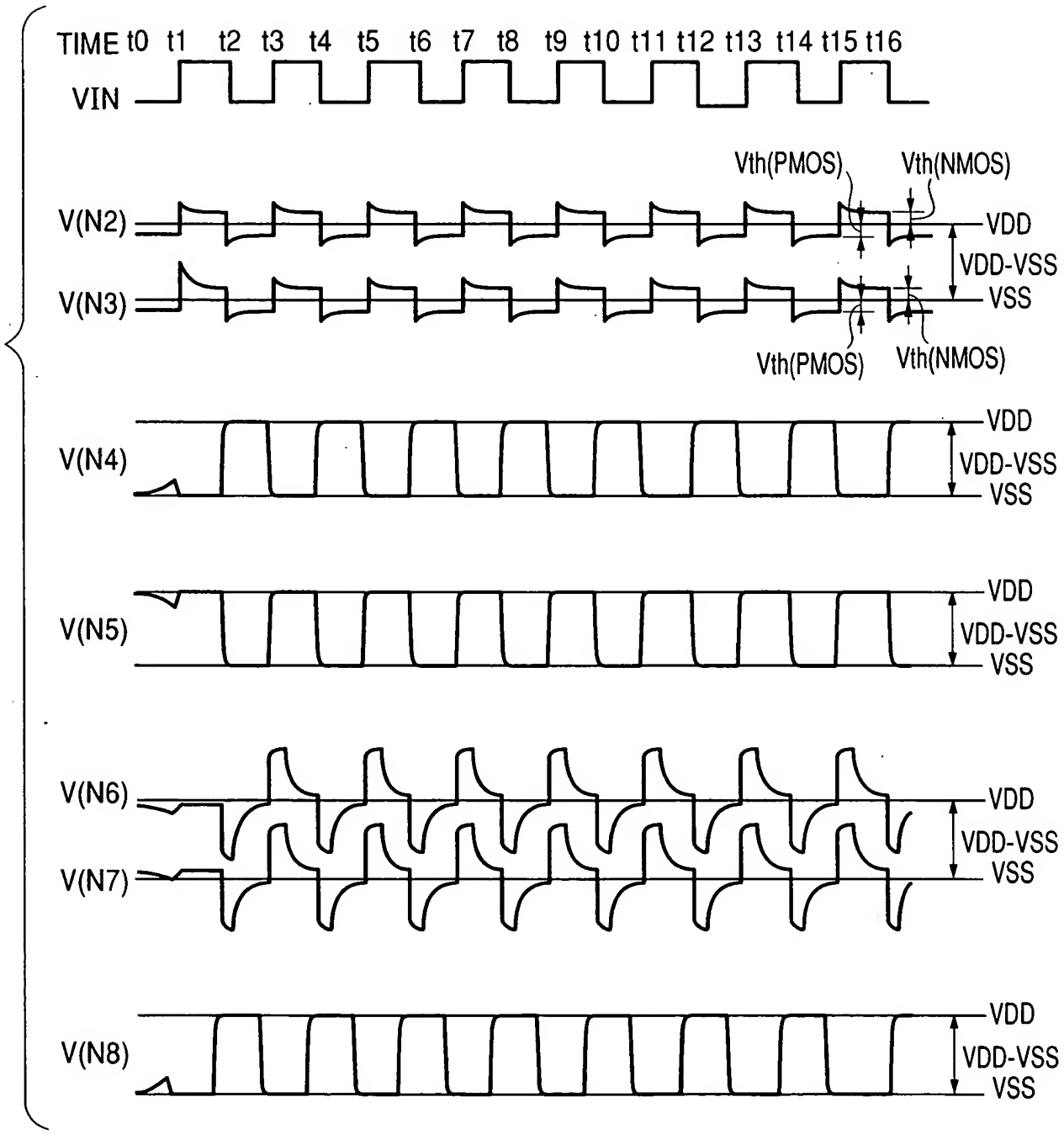
TIME t0 t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13 t14 t15 t16
VIN
Vth(PMOS)
Vth(NMOS)
V(N2)
VDD
VDD-VSS
V(N3)
VSS
Vth(PMOS)
Vth(NMOS)
V(N4)
VDD
VDD-VSS
VSS
V(N5)
VDD
VDD-VSS
VSS
V(N6)
VDD
VDD-VSS
V(N7)
VSS
V(N8)
VDD
VDD-VSS
VSS

FIG. 8A

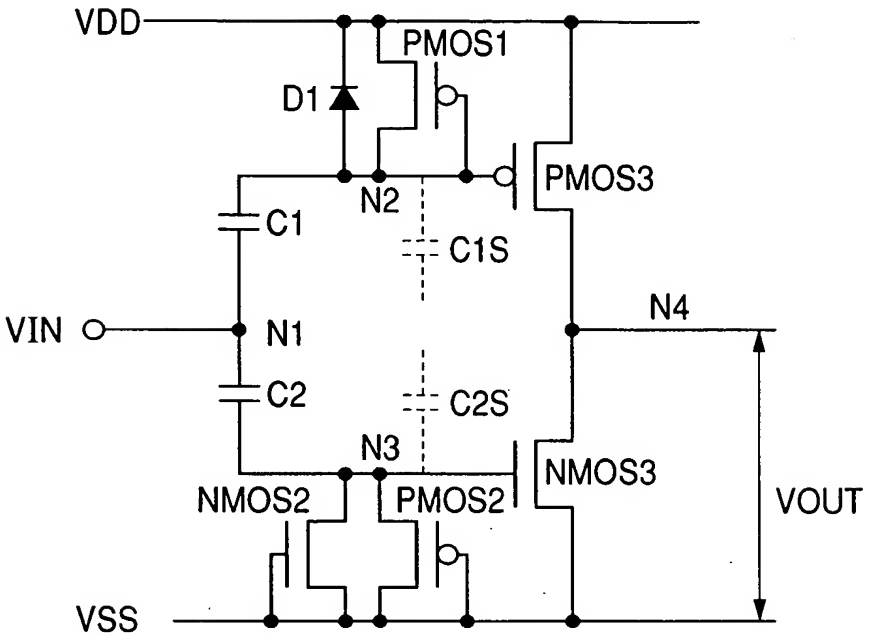
VDD
PMOS1
D1
PMOS3
N2
C1
C1S
VIN
N1
N4
C2
C2S
N3
NMOS3
NMOS2
PMOS2
VOUT
VSS

FIG. 8B

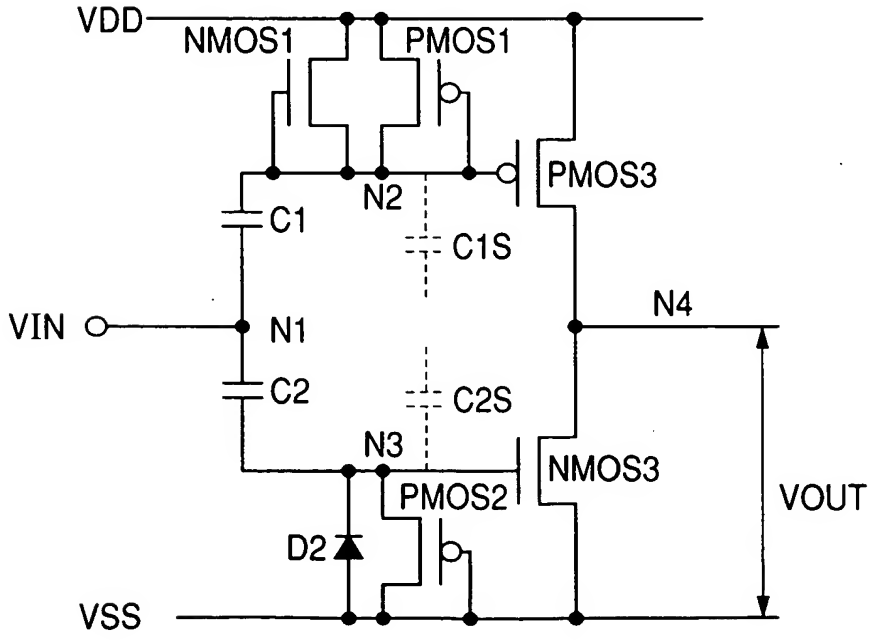
VDD
NMOS1
PMOS1
PMOS3
N2
C1
C1S
VIN
N1
N4
C2
C2S
N3
NMOS3
PMOS2
VOUT
D2
VSS

FIG. 8C

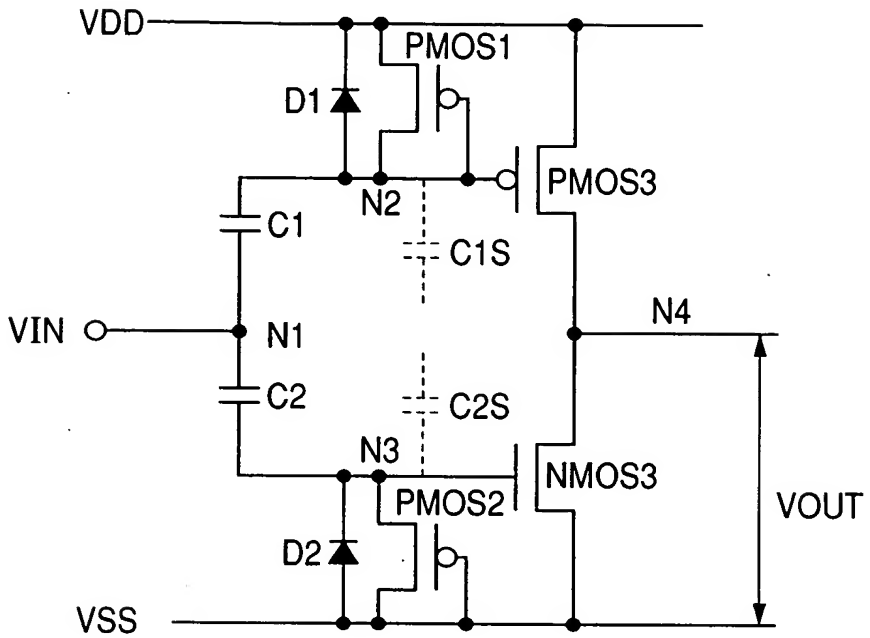
VDD
PMOS1
D1
PMOS3
N2
C1
C1S
VIN
N1
N4
C2
C2S
N3
NMOS3
PMOS2
VOUT
D2
VSS

FIG. 8D

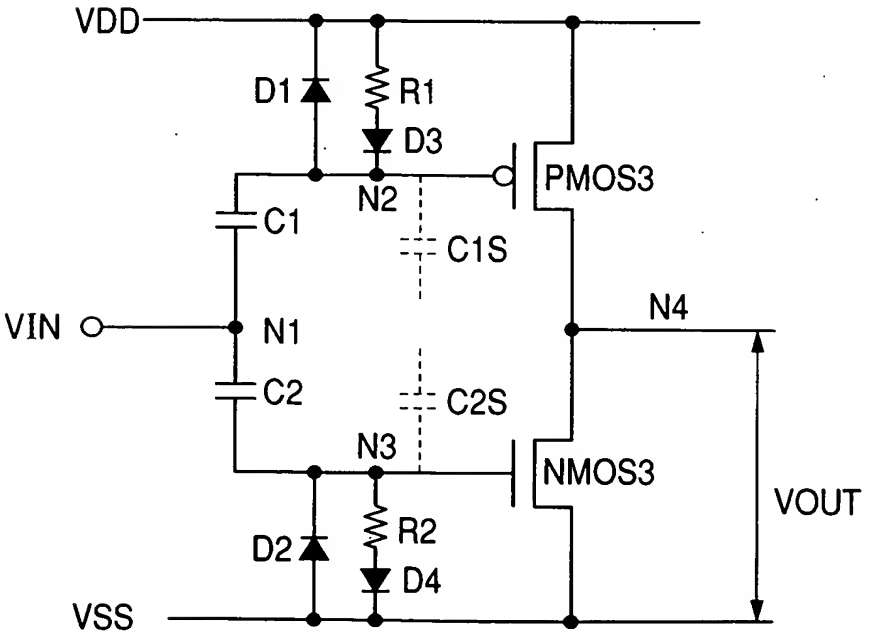
VDD
D1
R1
D3
PMOS3
N2
C1
C1S
VIN
N1
N4
C2
C2S
N3
NMOS3
VOUT
R2
D2
D4
VSS

FIG. 9A

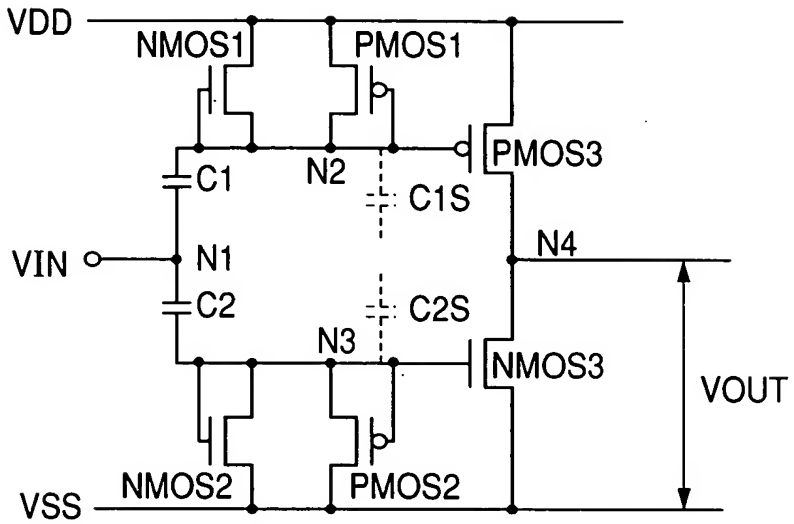

FIG. 9B

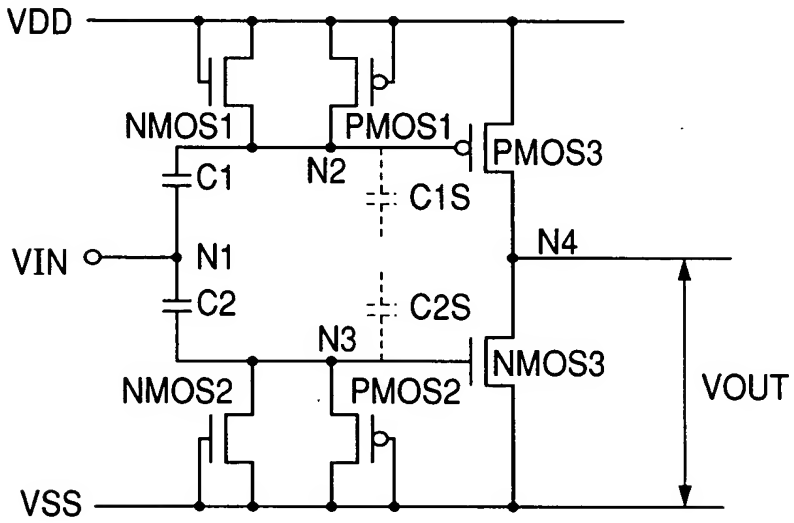

FIG. 9C

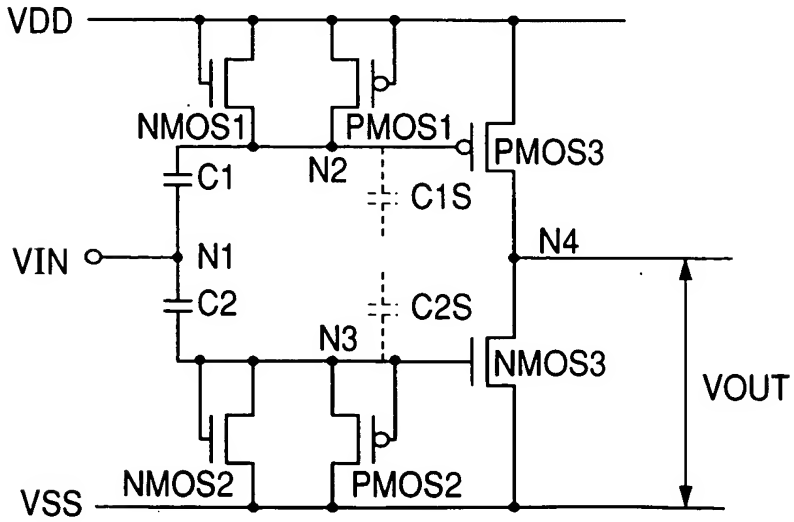

FIG. 10A

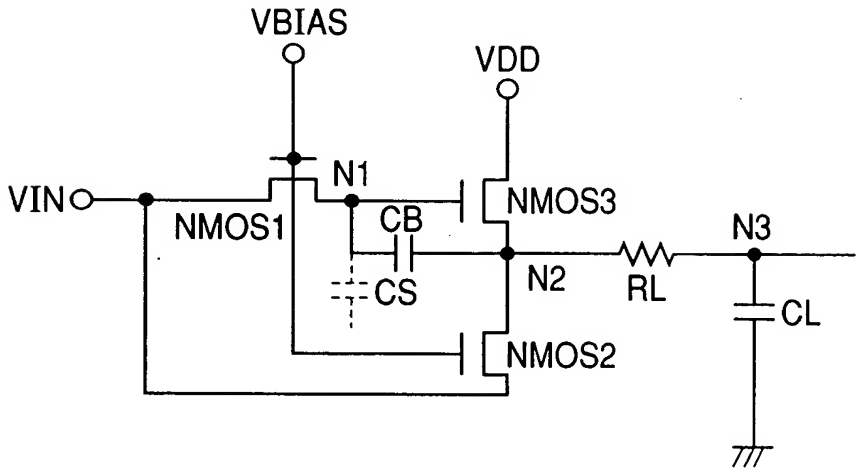

FIG. 10B

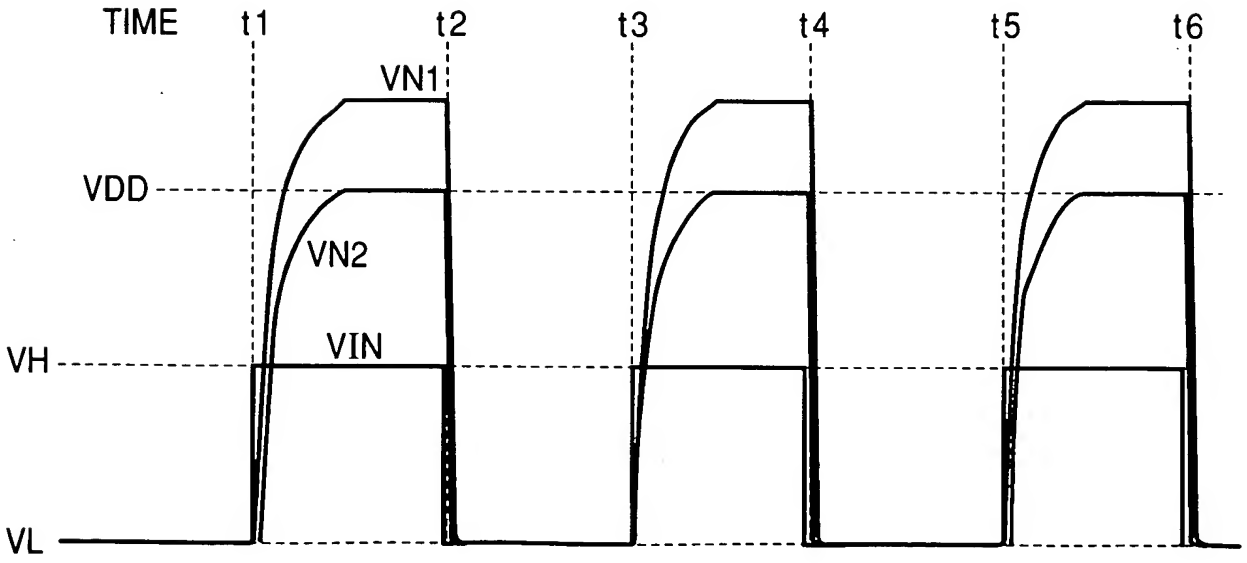

FIG. 11A

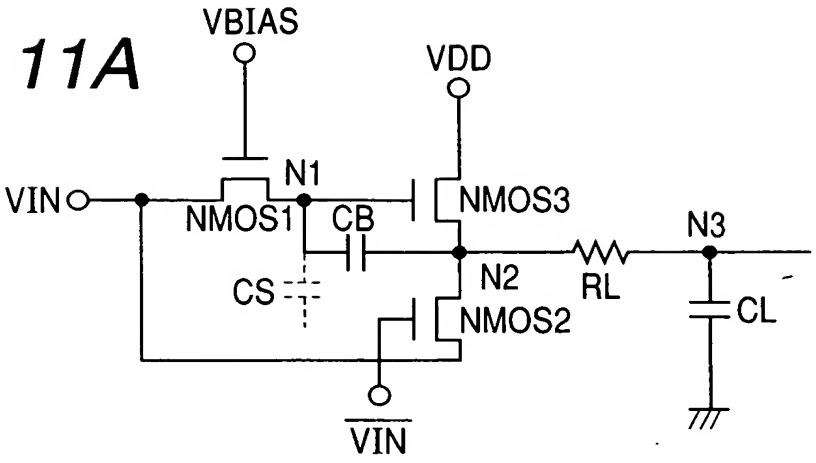

FIG. 11B

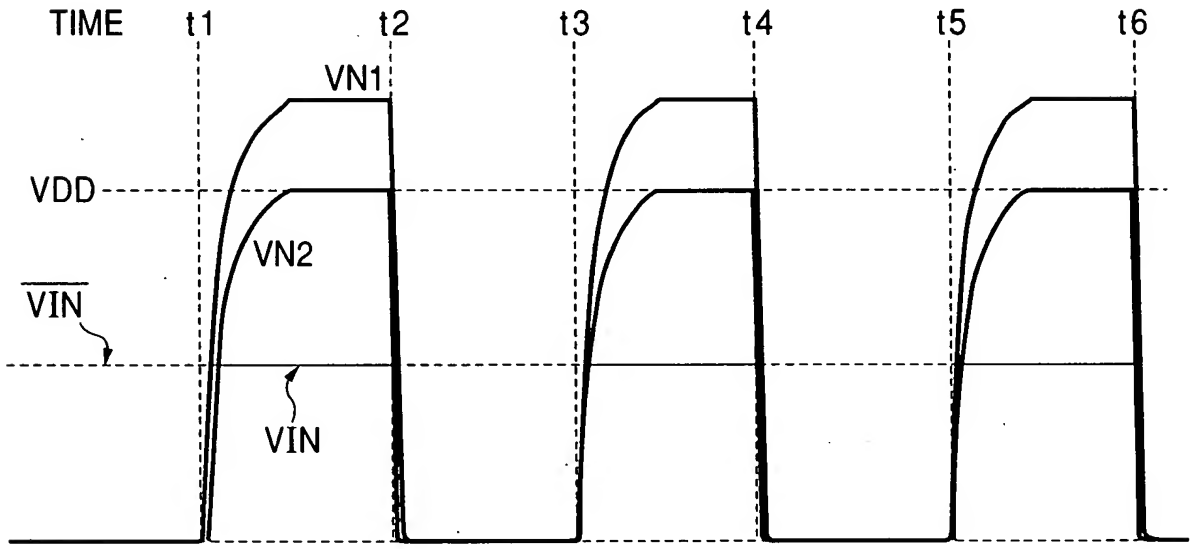

FIG. 11C

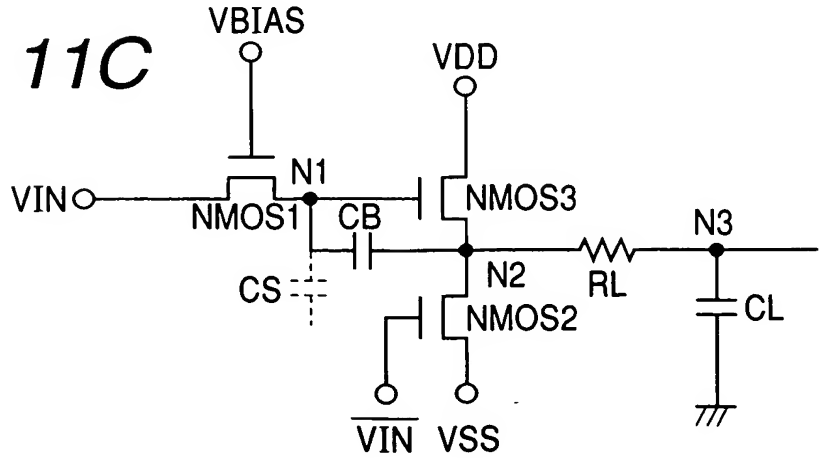

FIG. 12A

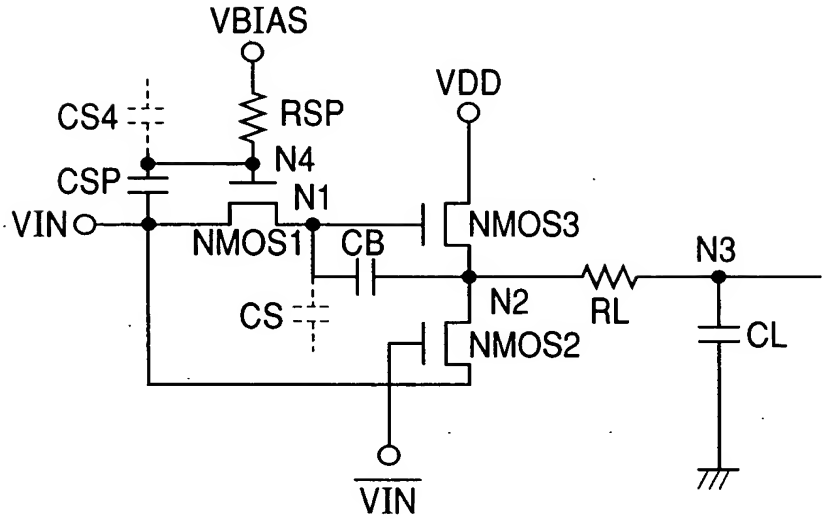

FIG. 12B

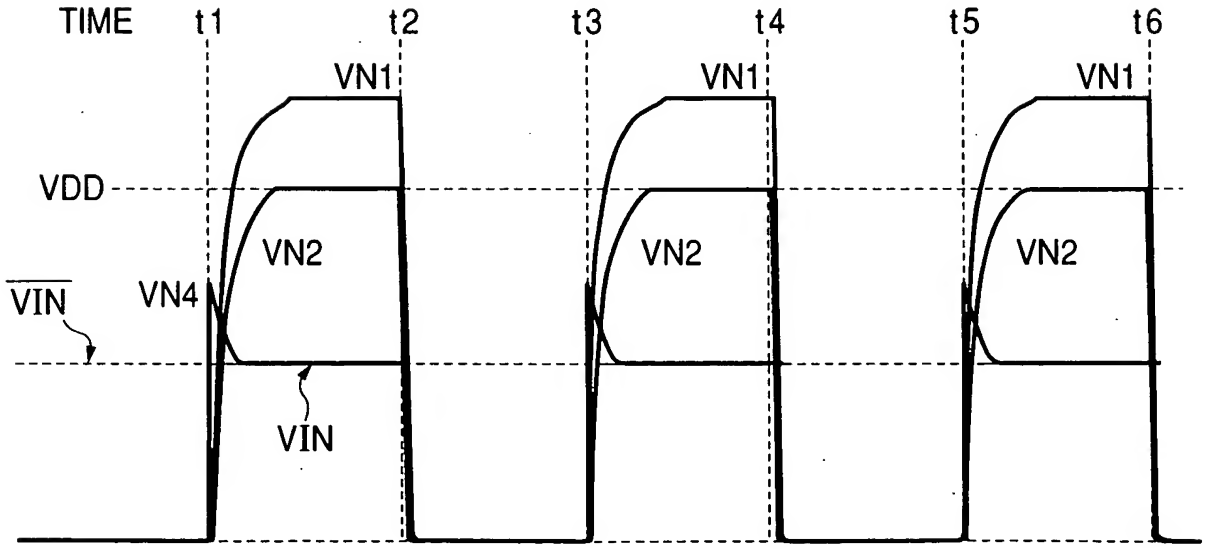

FIG. 13A

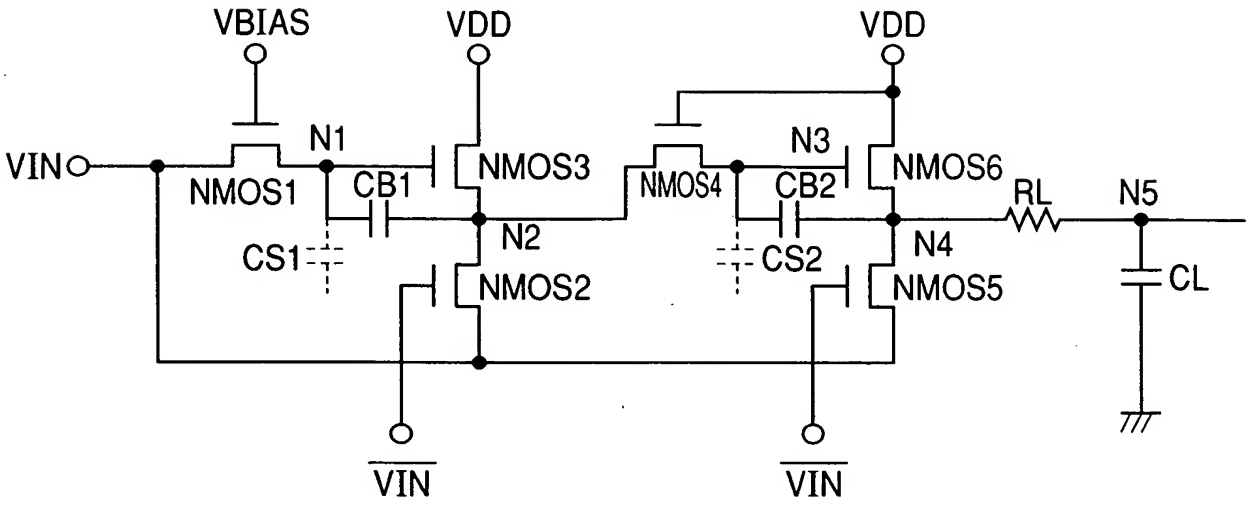

FIG. 13B

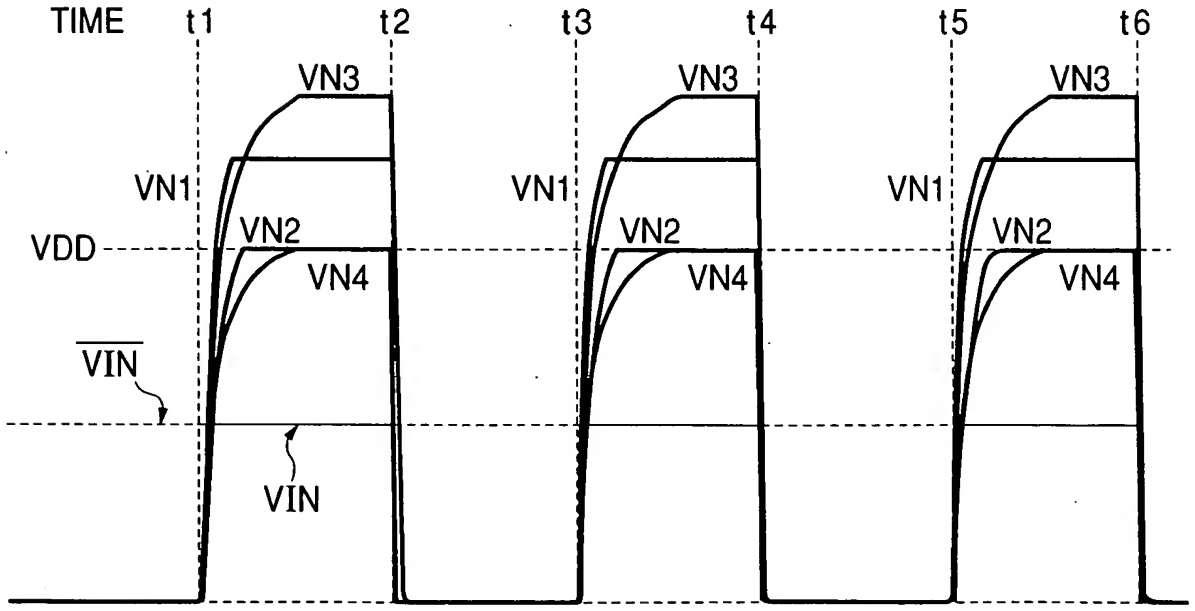

FIG. 13C

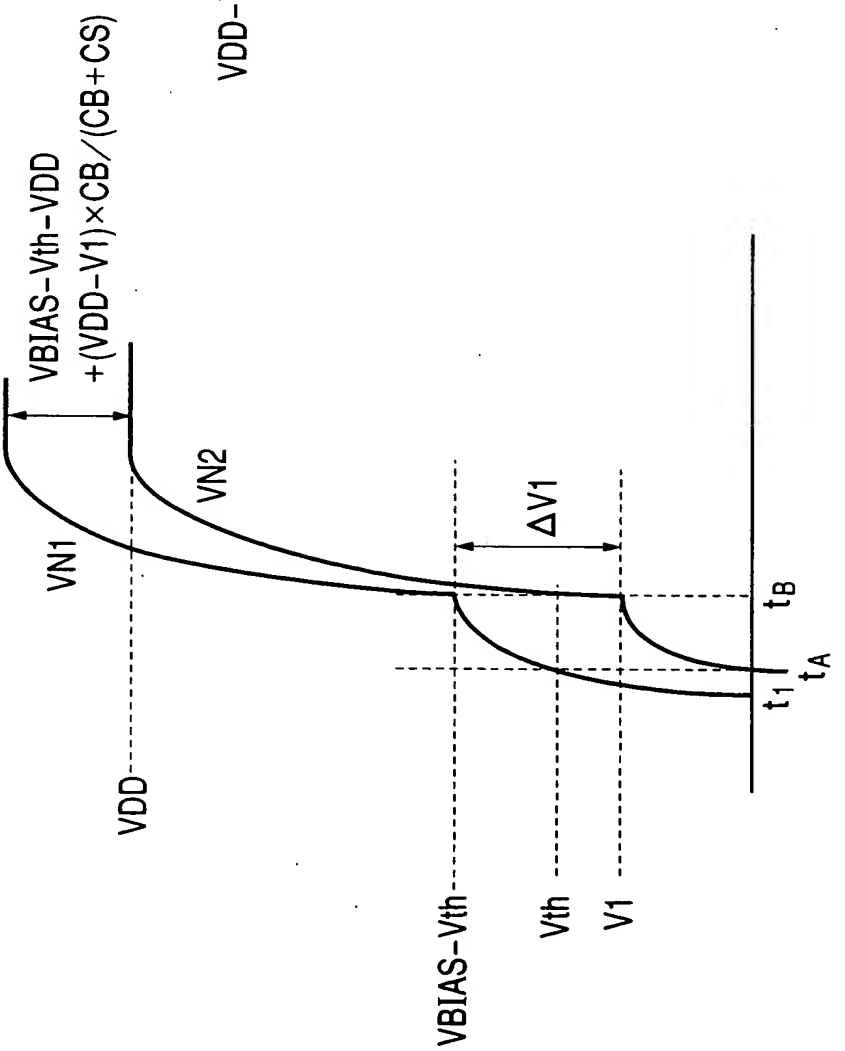

FIG. 13D

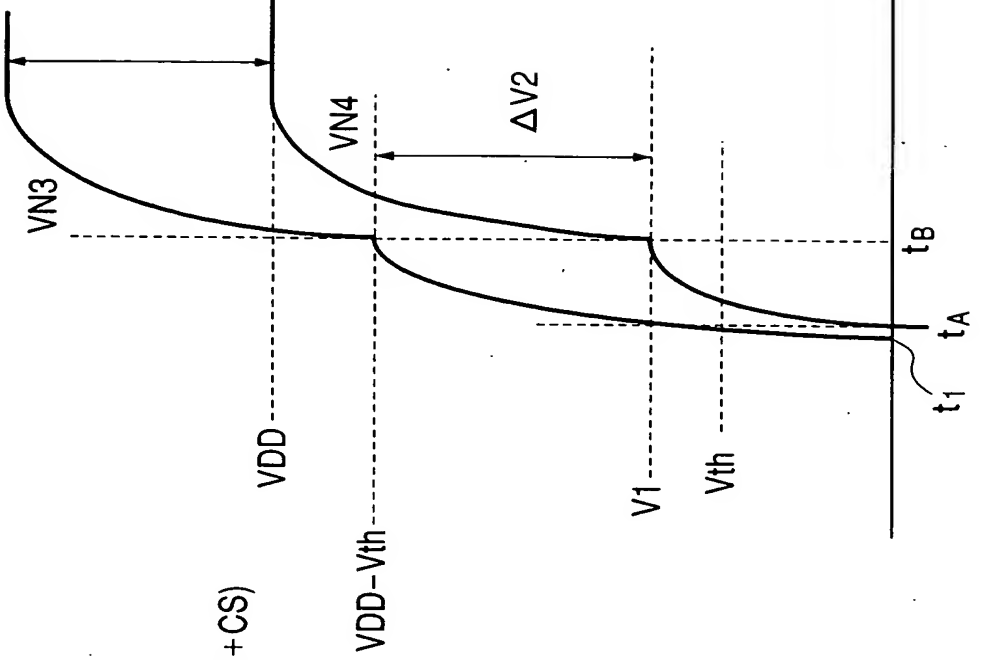

FIG. 14A

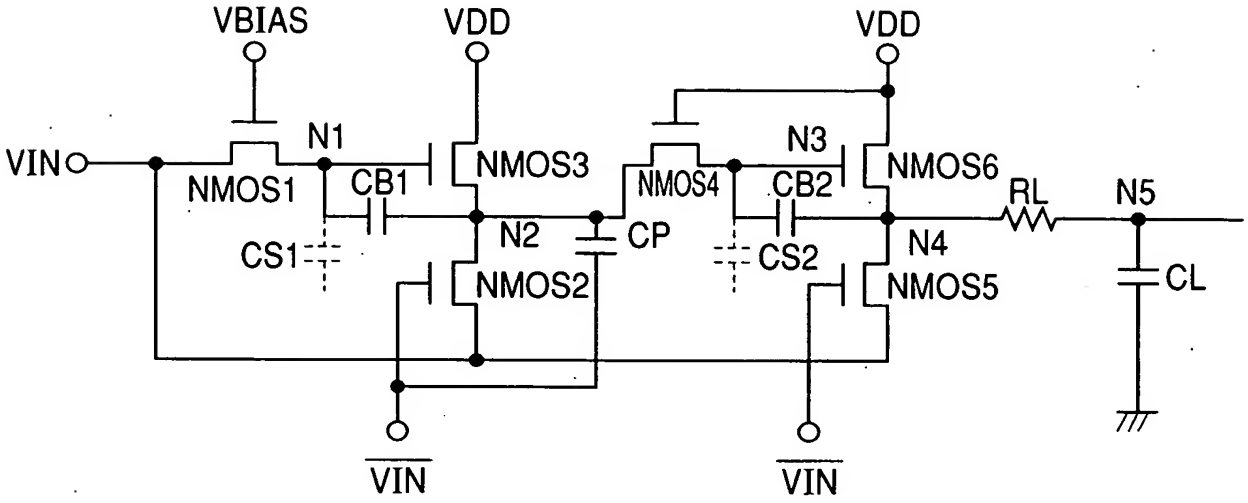

FIG. 14B

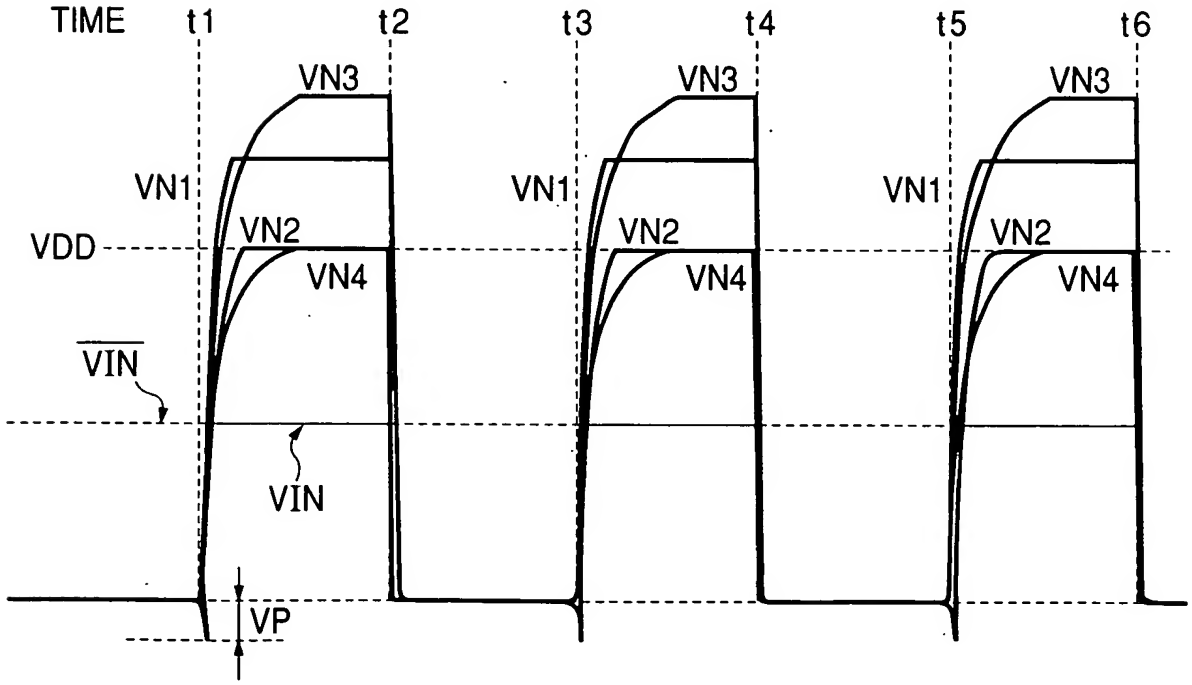

FIG. 14C

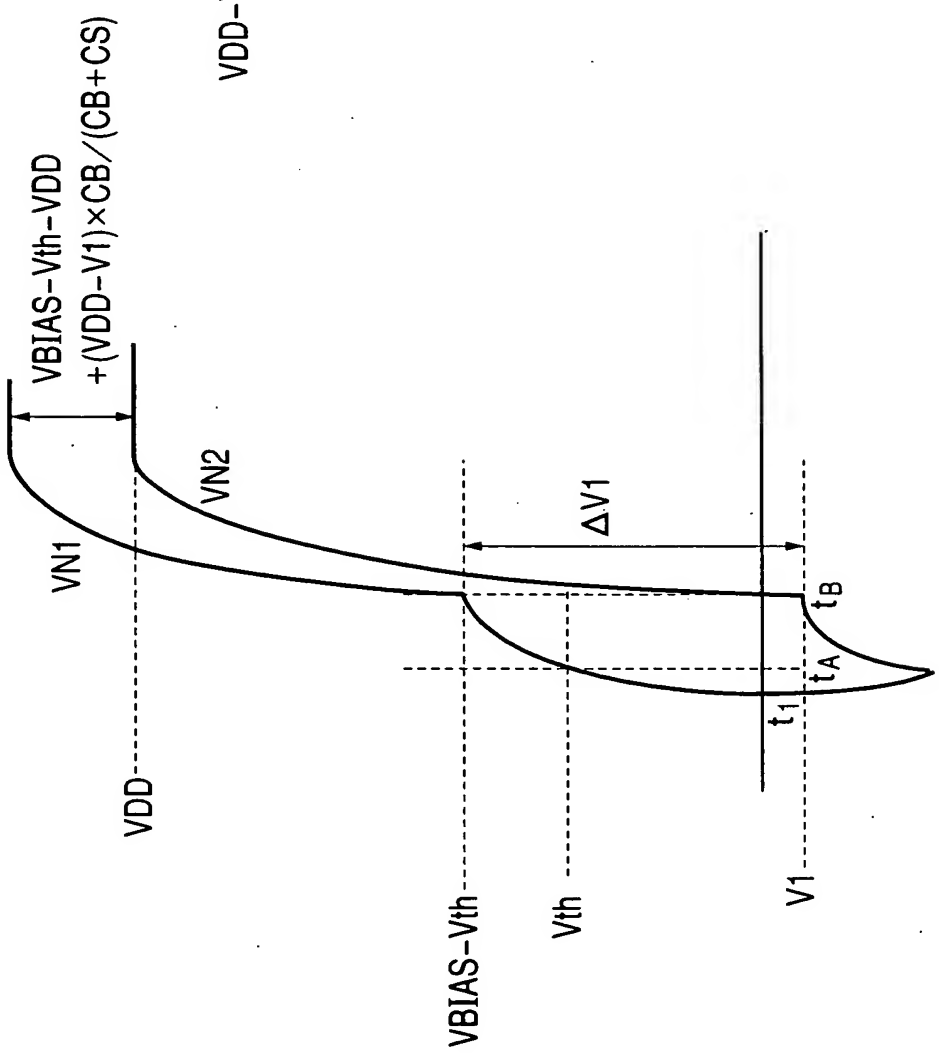

FIG. 14D

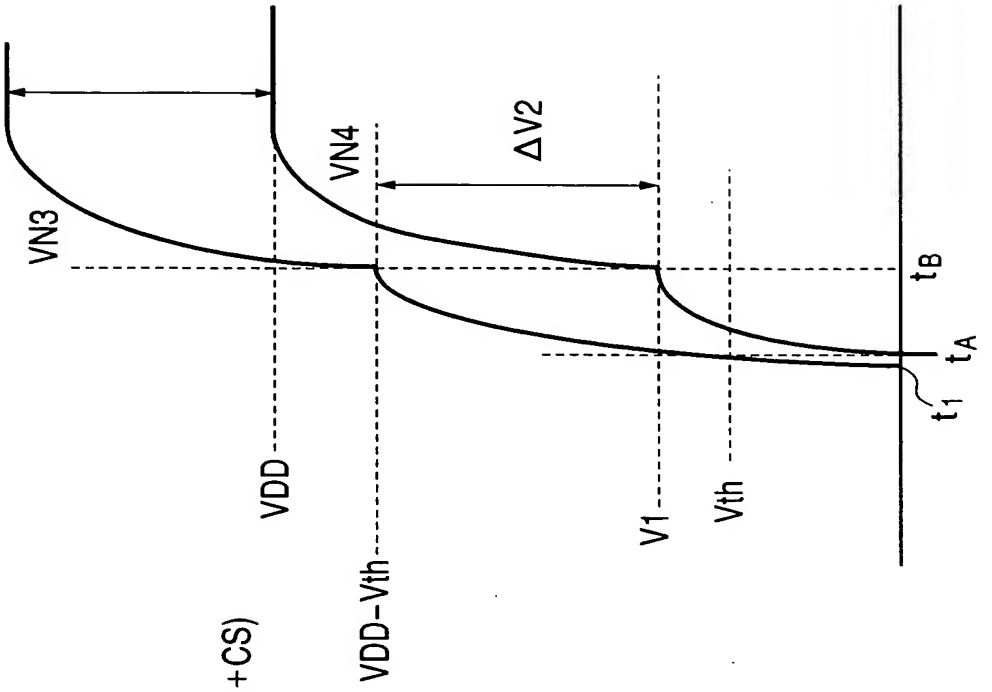

FIG. 15A

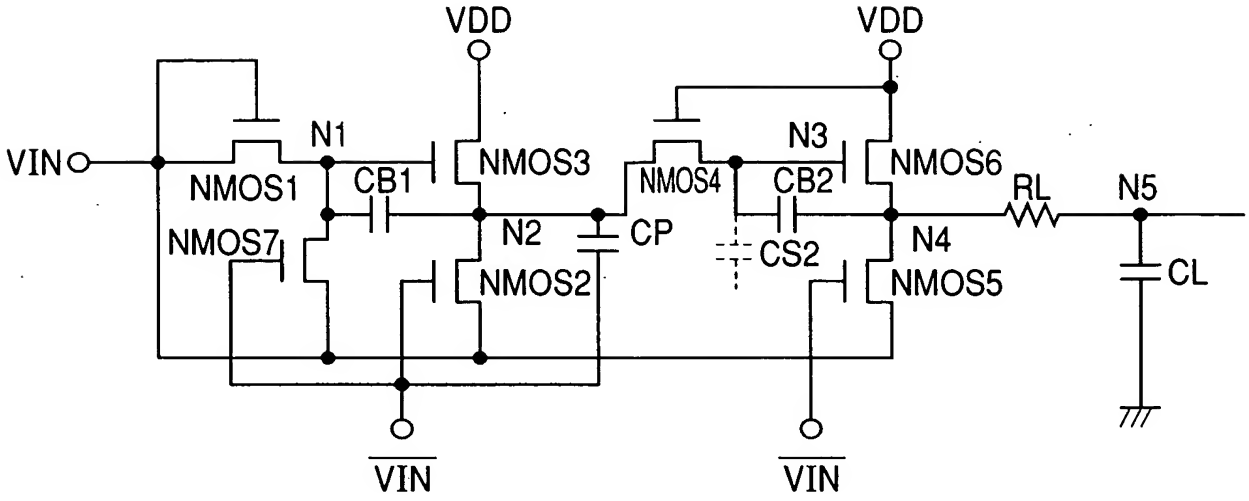

FIG. 15B

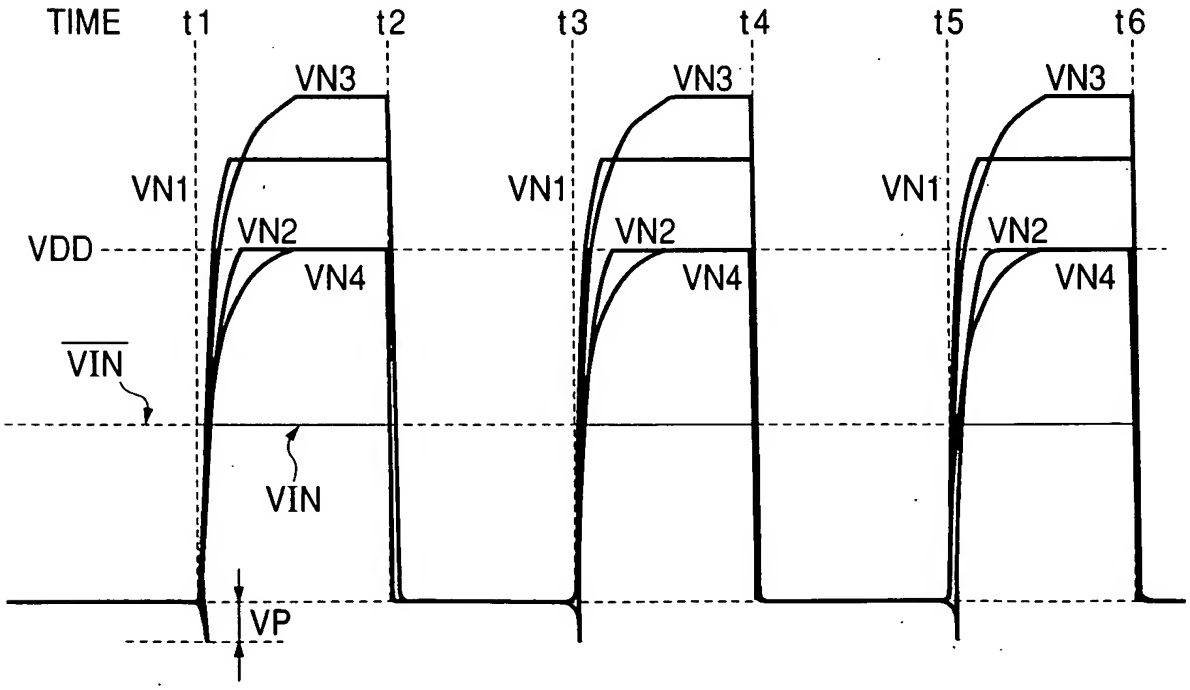

FIG. 15C

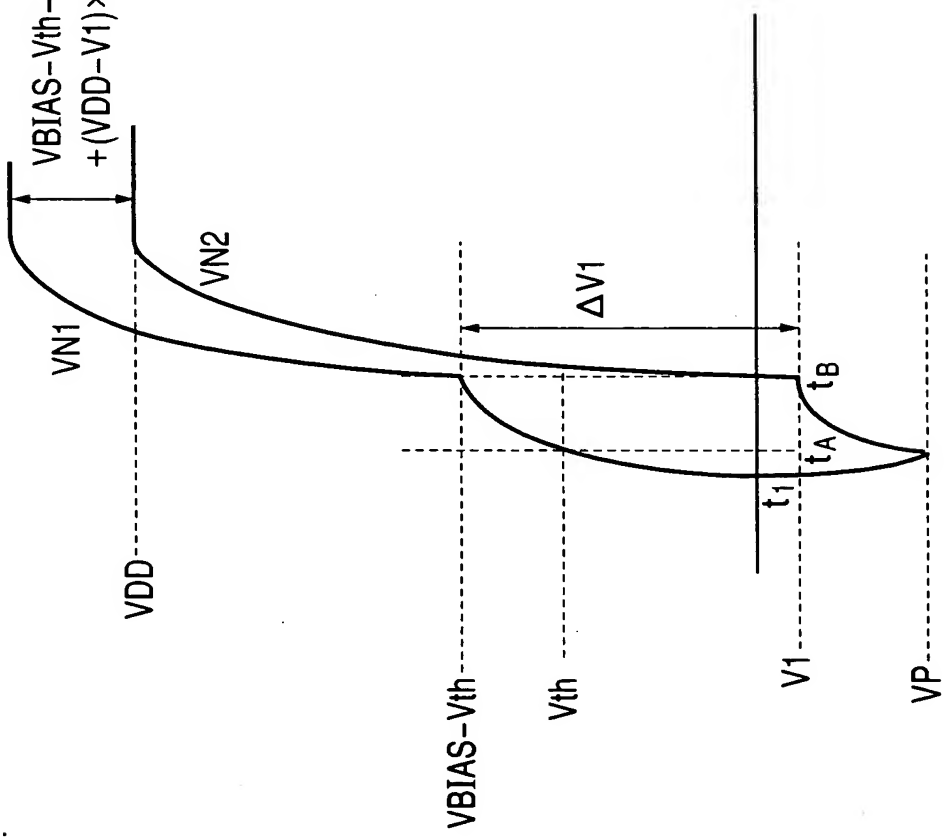

FIG. 15D

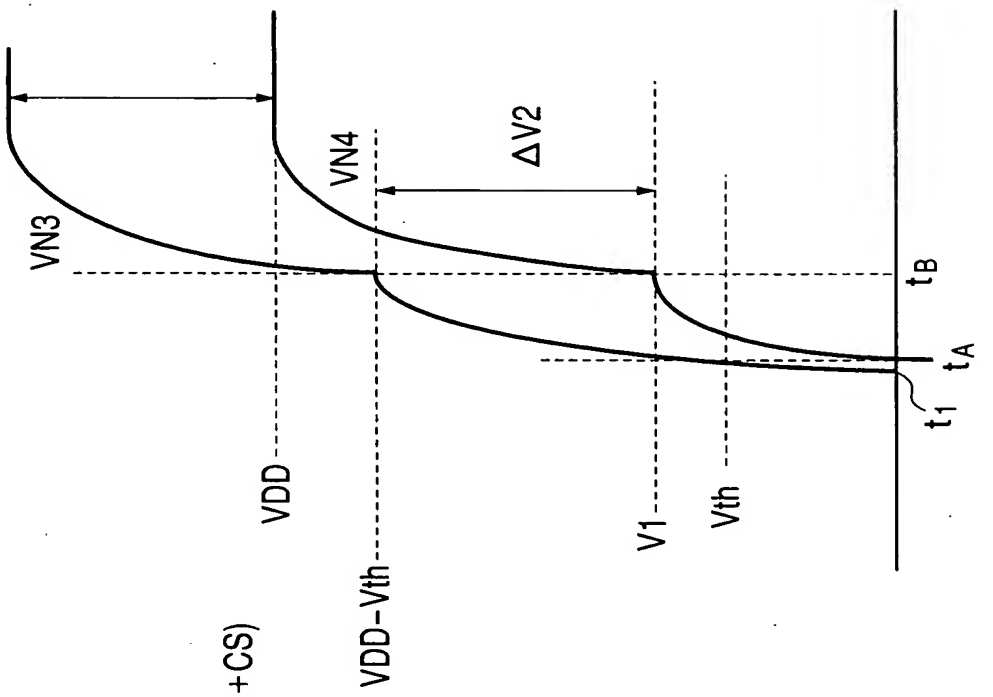

FIG. 16
PRIOR ART

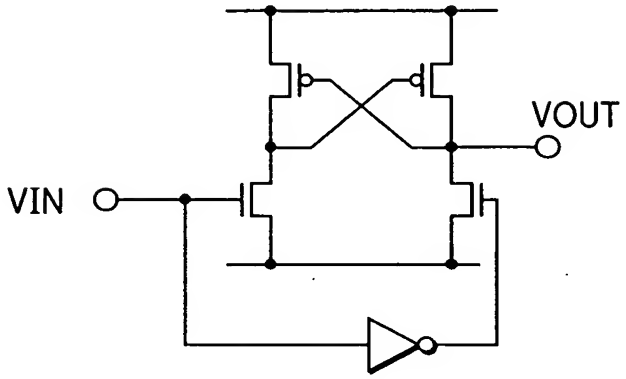

FIG. 17
PRIOR ART